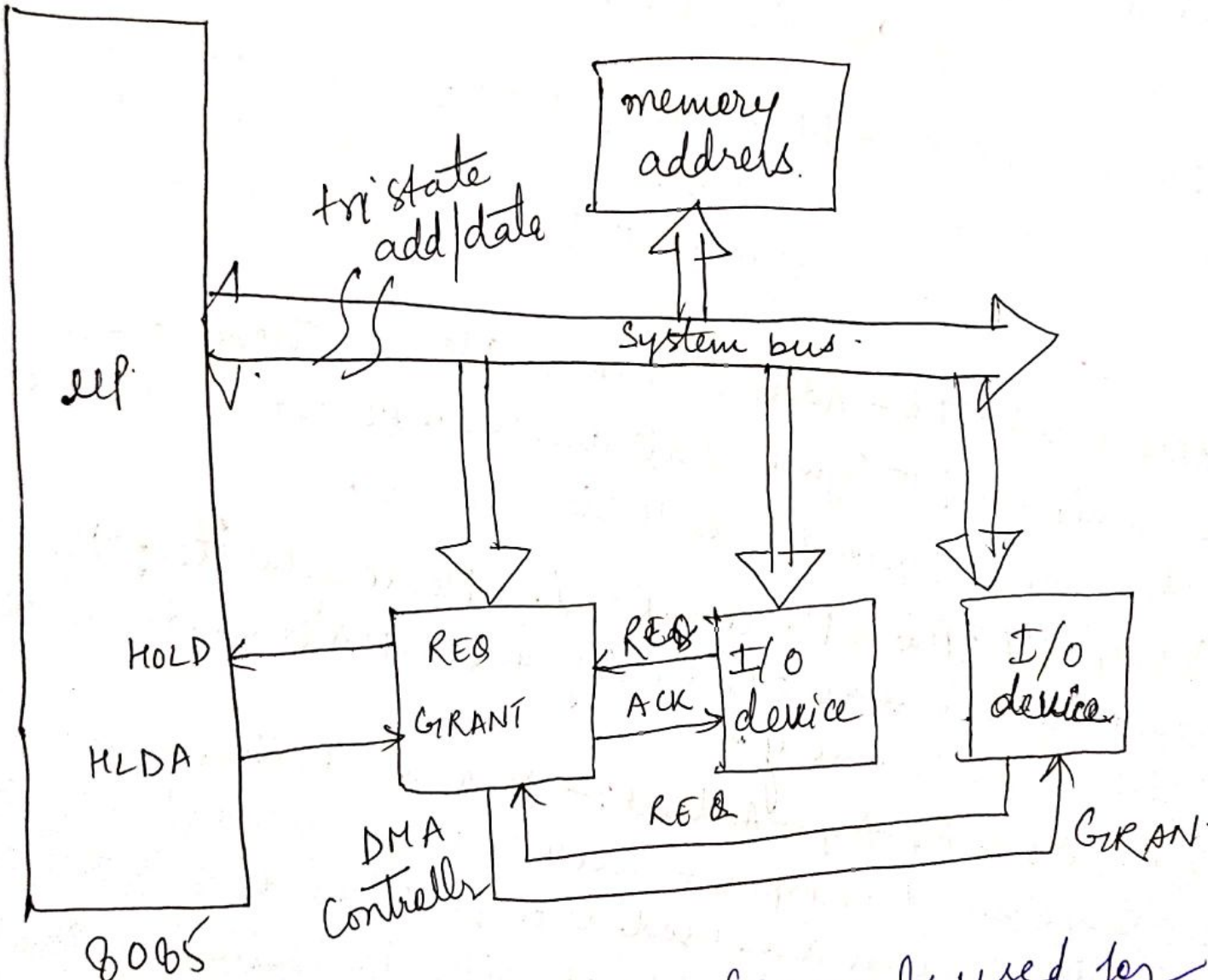
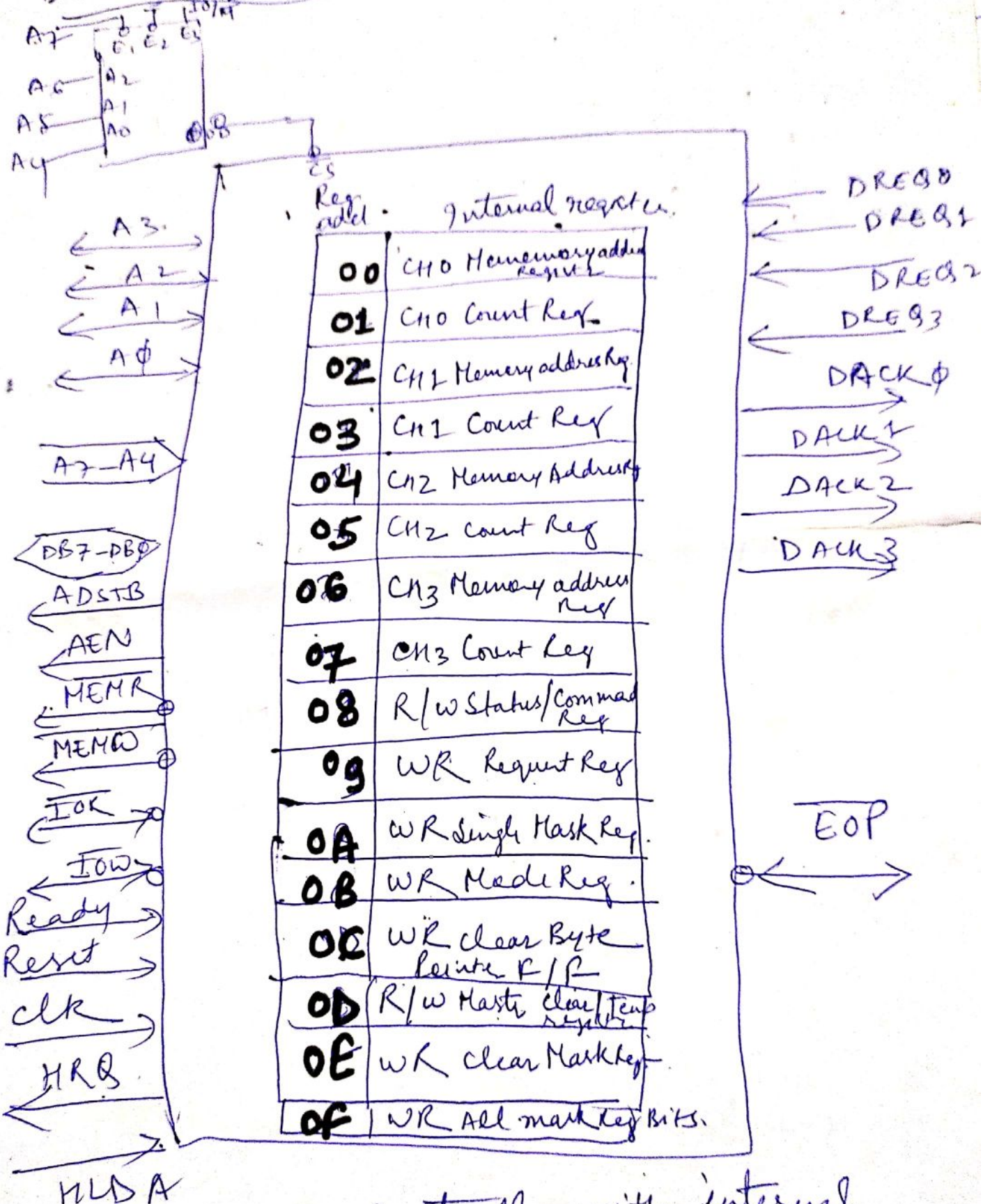
DMA Mode of Data Transfer



DMA is an I/O technique commonly used for high speed data transfer. for ex - between System memory & a floppy disk.

DMA Controller, 8237 DMA controller

Direct memory access



DMA Controller with internal registers.

DMA Signals → Signals are divided into two group :-
(1) one group of signals shown on the left of 8237 is used for interfacing with the MPU.
(2) The second group shown on the right-hand side of the 8237 is for communicating with peripherals.
The signals that are necessary to understand the DMA operation :-

1) DREQ0 - DREQ3 → DMA Request : These are four independent, asynchronous input signals to the DMA channels from peripherals such as floppy disks & hard disk, to obtain DMA service, a request is generated by activating the DREQ line of the channel.

2) DACK0 - DACK3 - DMA Acknowledge : These are output lines to inform the individual peripherals that a DMA is granted. DREQ & DACK are equivalent to handshake signals in I/O devices.

3) AEN and ADSTB - Address Enable & address strobe :- These are active high output signals that are used to latch a high order address byte to generate a 16 bit address.

4) $\overline{MEMR}$ & $\overline{MEMW}$ → Memory Read & Memory write : These are output signals used during the DMA cycle to write & read from memory.

5) A3-A0 & A7-A4 - Address :- A3-A0 are bidirectional address bus. They are used as inputs to access control registers. During the DMA cycle, these lines are used as output lines to generate a low-order address that is combined with the remaining lines A7-A4.

6) HRQ & HLDA → HRQ is an output signal used to request the MPU control of the system bus. After receiving the HRQ, the MPU completes the bus cycle in process & issues HLDA signal.

8237 is a programmable Direct memory Access Controller housed in a 40 Pin package. it has four independent Channels with each channel capable of transferring 64K bytes. it must interface with two type of devices:- MPU & the peripherals such as floppy disks.

DMA plays two roles in a given System:- it is an I/O to the microprocessor (Slave mode) & it is a data transfers processor to peripherals (master mode).

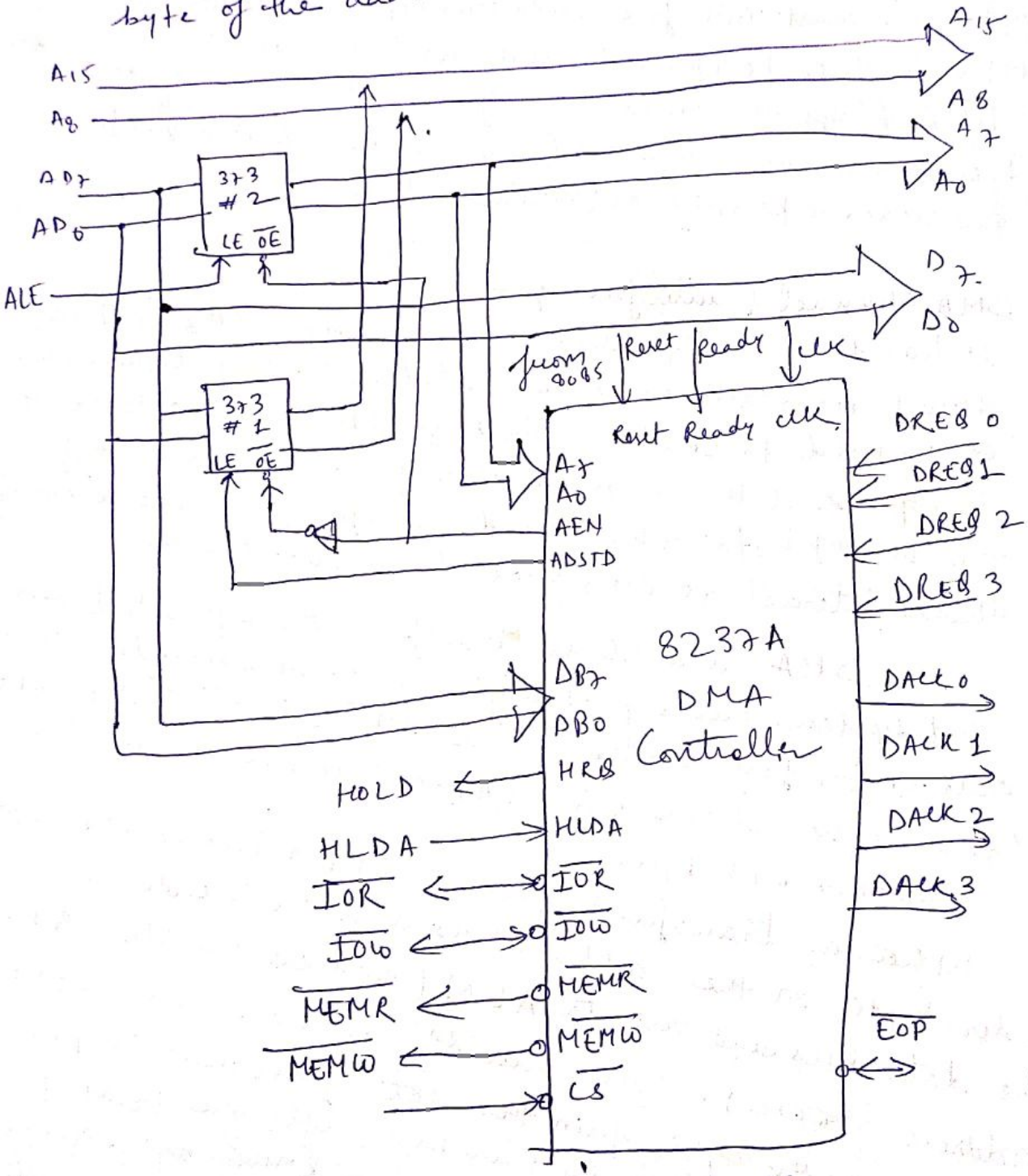
DMA channel & interfacing:-

It has four independent channels CH0 to CH3 internally two 16 bit registers are associated with each channel. one is used to load a starting address of the byte to be copied & the second is used to load a count of number of bytes to be copied. therefore, the addresses of these internal registers range from 00 to 0F.

DMA is used to transfer data bytes between I/O and system memory at high speed. it includes eight data lines, four control signals ($\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$ & $\overline{MEMW}$) and eight address lines (A7-A0) it needs 16 address lines to access 64K bytes.

When a transfer begins, the DMA places the low order byte on the address bus and high order byte on the data bus and asserts AEN (address Enable) ADSTB (address strobe). these two signals are used to latch the high order byte from the data bus; thus it places 16 bit address on the system bus. after the transfer of first byte latch is updated when lower byte generates a Carry. it uses two latches:- one to latch higher order address from the data bus by using AEN & ADSTB signals & the second latch to demultiplex the 8085 bus and generate the low order address bus by using the ALE signal.

AEN signal is connected $\overline{OE}$ signal of the second latch to disable the low order address bus from the 8085 when first latch is enabled to latch the high order byte of the address.



Interfacing 8237 - DMA Controller with 8085